REMARKS

Claims 11-18 and 26-35 are all the claims presently pending in the application. Claims 11-13 and 16-18 have been amended to more particularly define the invention. Claims 26-35 have been added to claim additional features of the invention. Attached hereto is a marked-up version of the changes made to the specification and claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claim 16 stands rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Claims 11-12 and 15 stand rejected under 35 U.S.C. § 102(e) as being unpatentable over Aozasa et al. (US Patent No. 6,054,734). Claims 11-14 and 17-18 stand rejected under 35 U.S.C. § 102(e) as being unpatentable over Durlam et al. (US Patent No. 5,940,319) and Bronner et al. (US Patent No. 6,242,770).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a microelectronic element array which includes a semiconductor substrate, a first dielectric layer formed on the substrate, a plurality of electrically isolated conductive regions disposed within the first dielectric layer, each conductive region comprising a conductive via, a second dielectric layer having a lower surface which is bonded to an upper surface of the first dielectric layer, and a plurality of semiconductor nodes formed in the second dielectric layer, each node being in electrical contact with the via.

Conventional devices do not include a diffusion barrier between the word line and a semiconductor node. As a result, the word line has to be made from high resistance refractory metal which is unreactive with the semiconductor material.

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The claimed invention, on the other hand, have conductive regions which include conductive vias. These vias may be formed, for example, of refractory metal. The via may act as a diffusion barrier which keeps the conductive region from reacting with the semiconductor material. Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum.

II. THE 35 USC §112, SECOND PARAGRAPH REJECTION

Claim 16 stands rejected under 35 U.S.C. §112, second paragraph as indefinite. Applicant notes, however, that this claim has been amended to address the concerns of the Examiner.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE PRIOR ART REFERENCES

A. The Aozasa Reference

The Examiner alleges that Aozasa teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Aozasa.

Aozasa discloses a non-volatile memory device in which the gate electrodes are formed on an upper surface and a lower surface of the channel via insulating layers, respectively, one used as a read electrode and the other used as a write electrode (Aozasa at Abstract).

However, Aozasa does not teach or suggest "*a plurality of semiconductor nodes formed in said second dielectric layer, each node being in electrical contact with said via*" as similarly recited in claim 1. As noted above, conventional devices do not include a diffusion barrier between the word line and a semiconductor node. As a result, the word line has to be made from high resistance refractory metal which is unreactive with the semiconductor material (Application at page 3, lines 3-9; page 8, lines 7-8).

The claimed invention, on the other hand, have conductive regions which include conductive vias (Application at Figure 5B). These vias may be formed, for example, of refractory metal. The via may act as a diffusion barrier which keeps the conductive region

from reacting with the semiconductor material. Therefore, a word line in the conductive region can be formed of a low resistance metal such as copper and aluminum (Application at page 8, lines 3-16).

Clearly Aozasa does not teach or suggest these novel features. Indeed, Aozasa is completely unrelated to the claimed invention.

Specifically, Aozasa discloses an insulating layer 206 and interlayer insulation 244 (Aozasa at Figure 10). In the insulating layer 206 is formed a semiconductor layer which includes a source region 220 and drain region 222 of a memory cell (Aozasa at col. 12, lines 22-29).

The Examiner seems to equate the gate electrodes 216 in the Aozasa device with the conductive regions of the claimed invention. However, the gate electrode 216 in Aozasa clearly does not include a conductive via. Further, in the claimed invention, the via may be in electrical contact with a semiconductor node (Application at Figure 5B). However, in Aozasa, the gate electrode 216 is merely in contact with the insulation 206 and the gate insulation 283d (Aozasa at Figure 23).

In addition, in the claimed invention, the semiconductor nodes may be formed in a second dielectric layer which may be bonded to first dielectric layer having the conductive regions. However, in Aozasa, the semiconductor layer (e.g., source and drain regions 220, 222) above the gate insulation 283 is formed in the same insulation 206 as the gate electrode 216 which the Examiner equates with the conductive regions of the claimed invention. Clearly, these devices are completely unrelated.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Aozasa. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Durlam and Bronner References

The Examiner alleges that Durlam would have been combined with Bronner to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Durlam discloses a magnetic random access memory (MRAM) which includes magnetic memory elements. A digit line and bit line are placed under and on top of the memory element. The lines are enclosed by a high permeability layer excluding a surface facing the memory element, which shields and focuses a magnetic field toward the memory element (Durlam at Abstract).

Bronner discloses a magneto-resistive memory cell which includes a substrate, monocrystalline diode formed in the substrate, a first conductor in the substrate and a second conductor formed above a magnetic tunnel junction formed on the diode (Bronner at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, the Durlam device is merely intended to prevent a magnetic memory element from thermal degradation during fabrication (Durlam at col. 1, lines 61-64), whereas Bronner is intended to minimize the resistance of a diode in a memory cell (Bronner at col. 3, lines 3-4). Clearly, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that "[i]t would have been obvious to form Durlam's diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes ... would provide high conductivity, high rectification, and low total resistance" which is insufficient to support the combination.

Moreover, neither of these references teach or suggest "*a plurality of semiconductor nodes formed in said second dielectric layer, each node being in electrical contact with said via*" as similarly recited in claim 1. As noted above, unlike conventional devices, the claimed invention has conductive regions which include conductive vias (Application at Figure 5B). These vias may be formed, for example, of refractory metal. The via may act as a diffusion barrier which keeps the conductive region from reacting with the semiconductor material. Therefore, a word line in the conductive region can be formed of a low resistance metal such as copper and aluminum (Application at page 8, lines 3-16).

Clearly, neither of these references teach or suggest these novel features. For example, the references fail to disclose a conductive region comprising a via. Indeed, in the Office Action, the Examiner completely failed to identify where either of these references disclosed such as via as in the claimed invention.

Specifically, in Durlam, the Examiner equates the digit line 82 with the conductive region in the claimed invention. However, nowhere does Durlam describe these digit lines 82 has including a conductive via.

Further, the metal conductor 82 in the Durlam device is formed of Al or Cu or their alloys (Durlam at col. 6, lines 36-38; col. 3, lines 35-38; Figures 3, 4 and 17). Thus, as shown in Figure 17, Durlam teaches forming the diodes 93 and 95 directly on the Al and Cu. As explained in the Application, Al and Cu is reactive with the semiconductor and therefore, the Durlam structure would result in an unreliable device. Indeed, one advantage provided by the conductive via in the claimed invention is that the via may act as a diffusion barrier to prevent a conductor such as Cu or Al from reacting with a semiconductor diode formed thereon. Therefore, contrary to the Examiner's allegations, Durlam does not teach or suggest the claimed invention.

Further, Bronner does not teach or suggest the novel features of the claimed invention. Referring to Figure 5B, Bronner may disclose a single crystal Si diode, but Bronner clearly does not form the diode in electrical contact with a via. Indeed, in Bronner, the diode 514 is in the shaped of a V-groove formed in an insulation layer100. A metal conductor 525 is formed on the diode 514 and an oxide layer 530 is formed on the metal conductor 525 (Bronner at Figure 5B). This is completely unrelated to the claimed invention. Thus, Bronner, does not make up for the deficiencies of Durlam.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

Applicant notes that claim 11 has been amended (e.g., "delectric" has been changed to "dielectric") to address the Examiner's objection thereto. Further, Applicant notes that the limitation claim 12 has been amended to recite "a plurality of nodes of [oriented single crystal grain, monocrystalline,] semiconductor material disposed within said upper layer of dielectric material" to address the Examiner's objection thereto.

In view of the foregoing, Applicant submits that claims 11-18 and 26-35, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 1/02/03

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims to read as follows:

11. (Amended) An array of microelectronic elements comprising:

[a)] a substrate of semiconductor material,

[b)] a lower layer of dielectric material disposed with a lower surface in contact with said substrate and an upper surface in spaced adjacency thereto,

[c)] a pattern of mutually electrically isolated metal conductors disposed within said lower layer of dielectric material, said metal conductors comprising a plurality of spaced apart conducting regions extending to said upper surface of said lower layer,

[d)] an upper layer of dielectric [delectric] material disposed with a lower surface thereof in contact with and bonded to said upper surface of said lower layer, and

[e)] a plurality of nodes of [oriented single crystal grain, monocrystalline,] semiconductor material disposed within said upper layer of dielectric material, each of said nodes being in electrical contact with only one of said conducting regions at said upper surface of said lower layer,

wherein each conducting region comprises a via comprising an electrically conducting material, each node being in electrical contact with said via.

12. (Amended) An array as set forth in claim 11, wherein each of said nodes comprises [comprising] a semiconductor device.

13. (Amended) An array as set forth in claim 11, wherein said semiconductor material comprises oriented single crystal grain, monocrystalline semiconductor material, and each of said nodes comprises [comprising] a diode.

16. (Amended) An array as set forth in claim 15 [12], wherein a first insulating layer is disposed over an upper surface of said upper layer and a second insulating layer is formed over said upper surface of said lower layer, and wherein a second gate electrode is deposited upon said first insulating layer above each field effect transistor.

17. (Amended) An array as set forth in claim 13 [11], wherein said oriented single crystal grain semiconductor material is oriented in the <100> orientation.

18. (Amended) An array as set forth in claim 11, wherein said electrically conducting material comprises at least one of W, Ti, and Ta [each conducting region comprises a via filled with electrically conducting material].